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Polygon Shaped Interconnect Bridge for Electronic Packages

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ABSTRACT

This disclosure describes the use of a polygon-shaped (polygonal) interconnect bridge for connecting chips within an electronic package. The polygon-shaped interconnect bridge can be made of film, silicon, or a combination of film and silicon structures. The polygon-shaped bridge can be customized to follow an outline perimeter of included chips and wiring and enables stacking of high performance chips. The polygon-shaped interconnect bridge enables avoidance of interconnect bridge overlap (collision) without any modifications to the floorplan, thereby providing cost and performance benefits. The interconnect bridge can be formed by sequential photo-patterning of multiple bridge layers. A boundary line is additionally photo-patterned for easy separation and release of the interconnect bridges from a main silicon wafer when all layers are completely formed. Polygonal interconnect bridges that include through silicon vias are singulated using backgrinding and plasma etching.

KEYWORDS

- Multi-die bridge
- Electronic packaging
- In-package interconnect
- Back grinding
- Polyimide film
- Through silicon via (TSV)
- Photo-patterning
- High Bandwidth Memory (HBM)

BACKGROUND

Interconnect bridges are commonly utilized to connect different chips within an integrated circuit (IC) package. Interconnect bridges are silicon based connecters that include routing layers that enable chip to chip transfer of power, communication signals, data elements, etc. However, when an interconnect bridge is utilized to connect chips that have a large offset, the interconnect bridge can interfere with other bridges or IP blocks on the chip, thereby posing challenges in manufacturing.

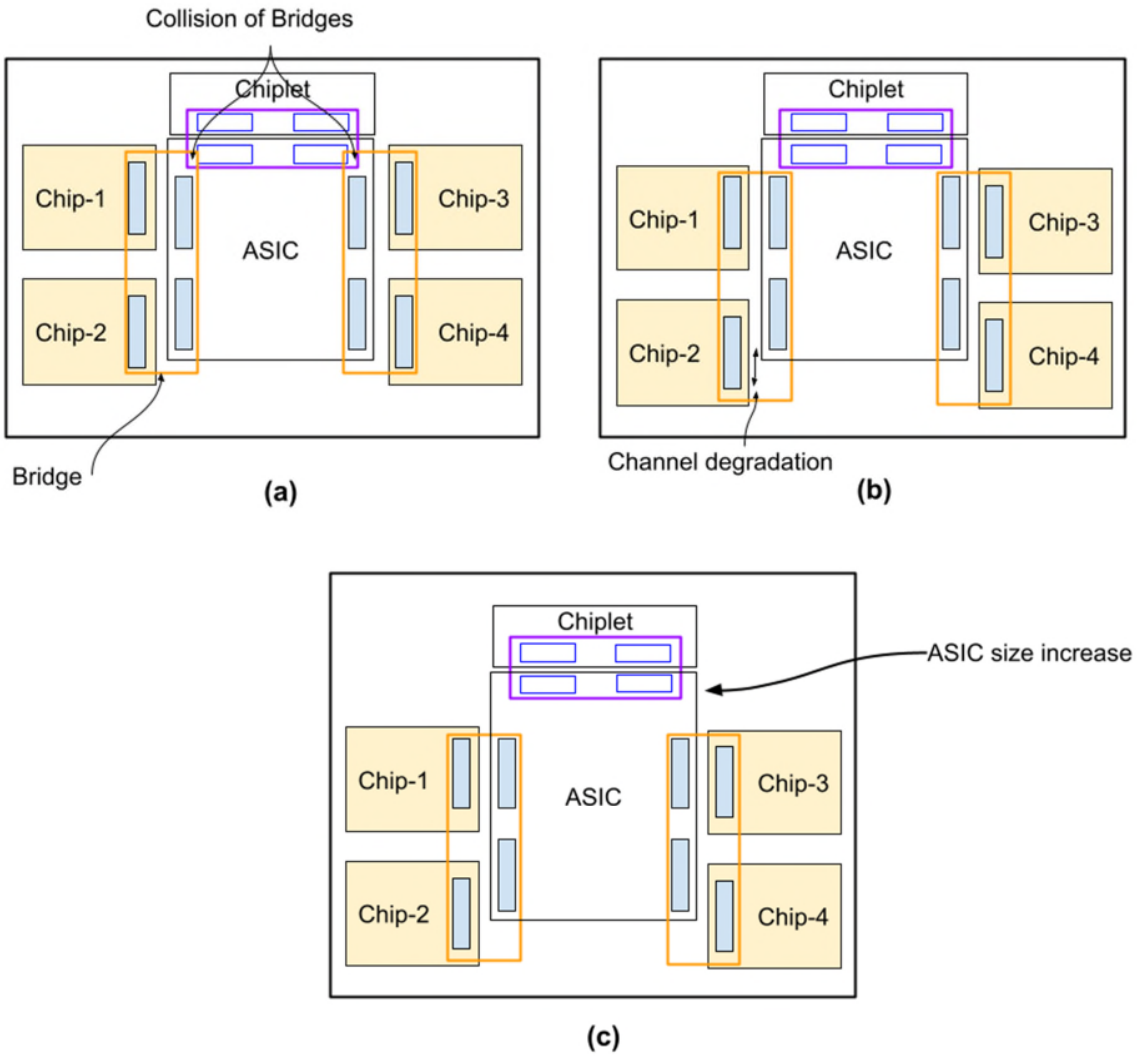

Fig. 1: Collision of bridge interconnects and example mitigation techniques

Fig. 1 illustrates some examples of issues that can be encountered with use of rectangular bridge interconnects. Fig. 1(a) depicts an example floorplan of a package that includes an application specific integrated circuit (ASIC), other chips, and a chiplet. Rectangular interconnect bridges are utilized to connect the ASIC to the chips and the chiplet. As depicted in Fig. 1(a), the layout of components causes the interconnect bridges to overlap, thereby posing manufacturing challenges as well as challenges to high speed input/output (HSIO) connections.

Fig. 1(b) depicts an example of mitigation of the problem wherein the layout is redesigned to shift the chips downward. While this can mitigate overlap (collision) of the interconnect bridges, the increased offset between the chip (e.g., Chip-2) and the ASIC can affect chip performance.

Fig. 1(c) depicts another example of mitigation of the problem wherein the ASIC silicon area is increased such that the bridge overlap is avoided. This comes with increased cost due to the increased silicon area.

DESCRIPTION

This disclosure describes a polygon-shaped (polygonal) interconnect bridge for connecting chips within an electronic package. The polygon-shaped interconnect bridges can be made of film, silicon, or a combination of film and silicon structures. The polygon-shaped bridge can be customized to follow an outline perimeter of included chips and wiring and enables stacking of high performance chips, e.g., high bandwidth memory (HBM), within a reasonable offset without the need to add additional silicon area.

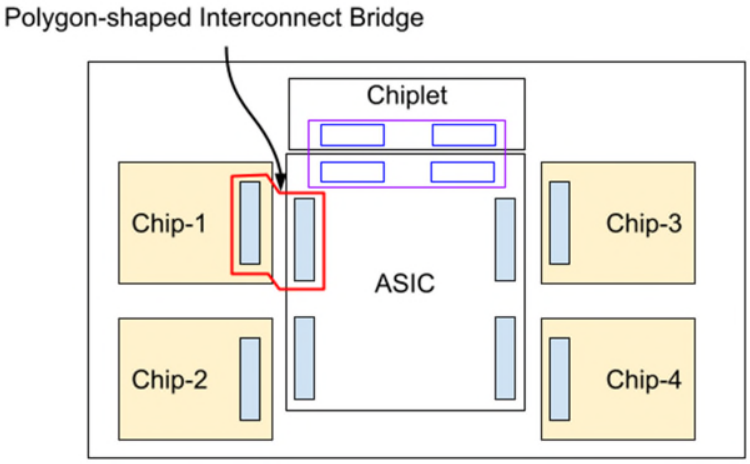

Fig. 2: A polygonal interconnect bridge is utilized to avoid bridge collision

Fig. 2 depicts use of an example polygonal interconnect bridge, per techniques of this disclosure. As depicted in Fig. 2, the polygon-shaped interconnect bridge enables avoidance of interconnect bridge overlap (collision) without modifications to the floorplan, thereby providing cost and performance benefits. The customized polygonal interconnect bridge is designed such that it can connect the intended components (e.g., chip and ASIC) and avoids other components in the package.

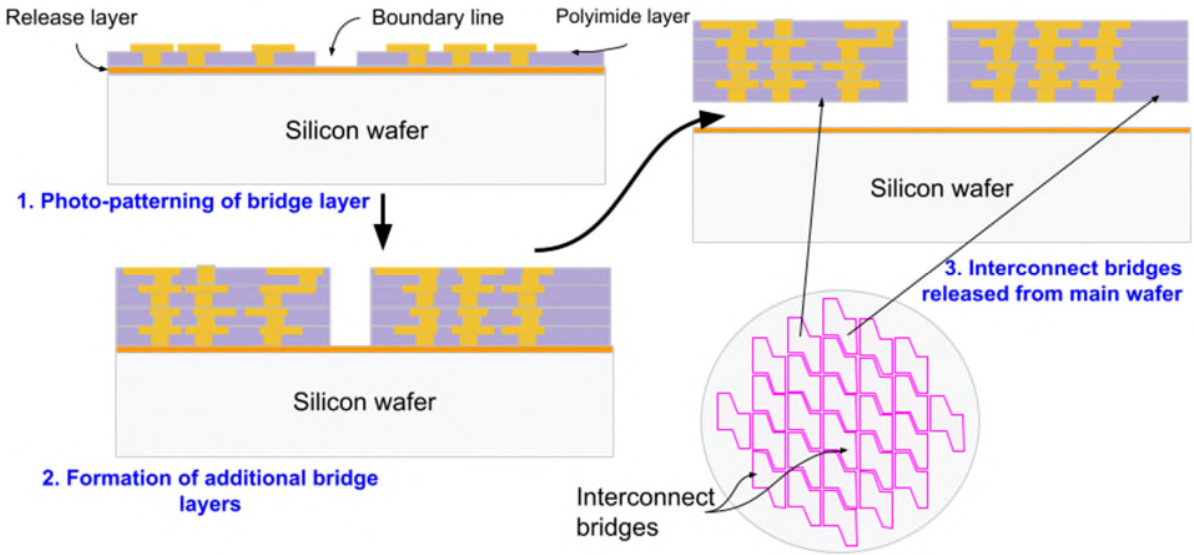

Fig. 3: Process flow for fabrication of interconnect bridges

Fig. 3 illustrates an example process flow for the fabrication of polygonal interconnect bridges, per techniques of this disclosure. As depicted in Fig. 3, an interconnect bridge is formed by sequential photo-patterning of multiple bridge layers. In some implementations, a polyimide film is utilized for the interconnect bridge. A boundary line is additionally photo-patterned for easy separation and release of the interconnect bridges from a main silicon wafer when all layers are completely formed.

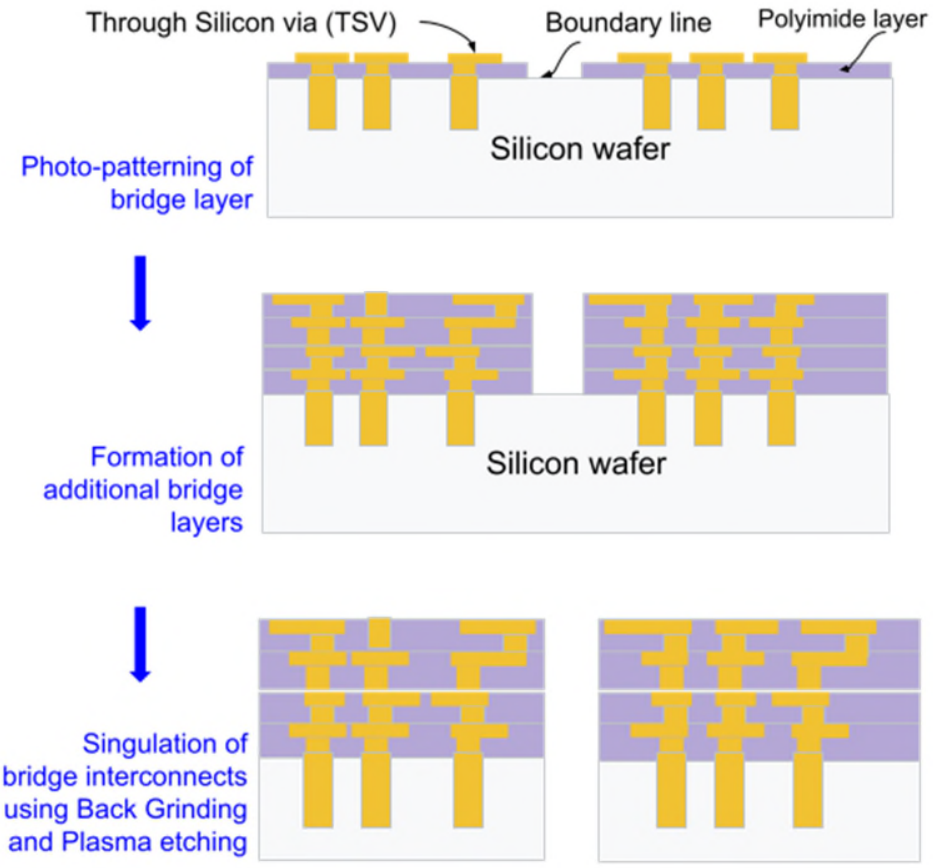

Fig. 4: Fabrication of polygonal interconnect bridges that include TSVs

Fig. 4 illustrates an example process flow for the fabrication of polygonal interconnect bridges that include through silicon vias (TSV), per techniques of this disclosure. As depicted in Fig. 4, multiple layers of the interconnect bridge are formed over the silicon wafer. The TSV

connections extend from the silicon wafer and through the bridge layers. When the bridge layers are completely formed, singulation of the interconnect bridges is performed using a backgrinding and plasma etching (dry etch) process.

CONCLUSION

This disclosure describes the use of a polygon-shaped (polygonal) interconnect bridge for connecting chips within an electronic package. The polygon-shaped interconnect bridge can be made of film, silicon, or a combination of film and silicon structures. The polygon-shaped bridge can be customized to follow an outline perimeter of included chips and wiring and enables stacking of high performance chips. The polygon-shaped interconnect bridge enables avoidance of interconnect bridge overlap (collision) without any modifications to the floorplan, thereby providing cost and performance benefits. The interconnect bridge can be formed by sequential photo-patterning of multiple bridge layers. A boundary line is additionally photo-patterned for easy separation and release of the interconnect bridges from a main silicon wafer when all layers are completely formed. Polygonal interconnect bridges that include through silicon vias are singulated using backgrinding and plasma etching.